

Best Practical Jitter Tolerance Testing with MP1900A

Signal Quality Analyzer-R MP1900A

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1. Introduction

The recent improvement to semiconductor device performance has seen bit rates of 28 Gbps become commonplace. When using high-speed signals like the 28 Gbps band, the impact of jitter components from various sources in the surrounding environment on the transmission quality cannot be ignored. As a result, accurate evaluation of device characteristics requires testing by injecting multiple types of jitter on the device under test (DUT). Previously, jitter tolerance tests for the optical market required only applying of sinusoidal jitter (SJ). More recently, applying just SJ has caused difficulties in performing accurate evaluation of device characteristics including the impact of the surrounding environment. This Application Note explains each type of jitter, gives some guidance about measurements for complex jitter tests, and describes some concrete examples of jitter tolerance measurements using the Anritsu MP1900A.

2. Definition of Jitter Component Types

2.1 SJ (Sinusoidal Jitter)

Sinusoidal Jitter is jitter with a single frequency component; it is the most basic jitter component of jitter tolerance tests. There are various jitter frequency components in the natural world and SJ is used for confirming the jitter tolerance at each frequency.

In transmission methods where the Data and Clock are not transmitted in parallel, the Data signal generated from the transmitting device is retimed by the Clock Recovery circuit at the receiving device. The jitter tolerance characteristics are a key index in evaluating this re-timing operation. Generally, Clock Recovery uses an internal Phase Locked Loop (PLL) circuit. Figure 2.1.1 shows a Clock Recovery circuit.

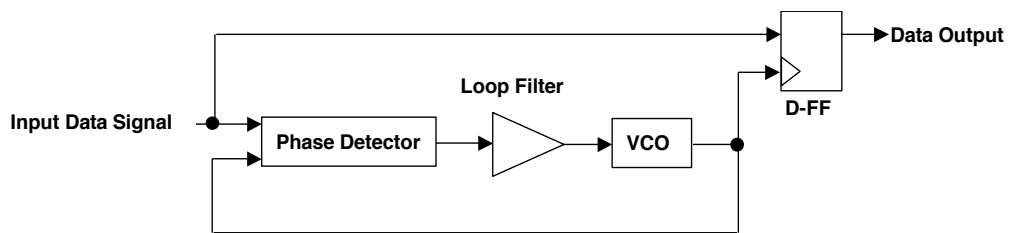


Figure 2.1.1 Clock Recovery Circuit

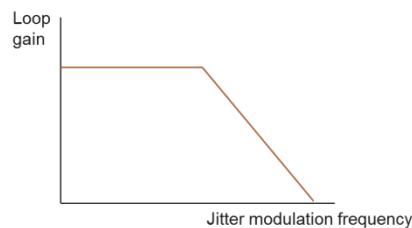


Figure 2.1.2 Loop Bandwidth

Similar to a basic PLL circuit, the Clock Recovery circuit determines the Loop Bandwidth (Figure 2.1.2). When the Loop Bandwidth is wide, the jitter tolerance is excellent; a shorter Clock Recovery circuit lock time has merits but on the other hand it increases the amount of carrier jitter in circuits downstream of the Clock Recovery. If the Clock Recovery lock time is short so as to recover the normal signal status, only a short time is required until the entire system recovers normal operation when the signal input to the Clock Recovery is lost or when the frequency has slipped momentarily. Although a wide loop band achieves this short lock time, a disadvantage is that jitter in the input clock is easily transferred to circuits downstream of the Clock Recovery. For example, stacking-up several wide Loop Bandwidth Clock Recovery circuits may cause jitter summing in subsequent stages, risking incorrect operation of the entire system.

At a jitter tolerance test, it is important to confirm that the Loop Bandwidth of the above-described PLL is in accordance with the design and the degree to which it varies; as already described, the Clock Recovery has its own unique Loop Bandwidth. When the input Data signal jitter frequency and amount are within the Loop Bandwidth, an error does not occur due to a phase mismatch because recovered clock tracks input Data signal in terms of jitter. In other words, for the input Data and recovered Clock to have the same amount of jitter, the relationship between the Clock and Data at D-FF in Figure 2.1.1 must be maintained so that no errors occur.

However, when the jitter in the input signal is out-of-band, the recovered Clock jitter is suppressed to be smaller than the jitter in the input Data signal. As a result, the relationship between the Clock and Data at D-FF in Figure 2.1.1 is changed and an error occurs.

SJ is the most basic jitter component used at the jitter tolerance test for confirming the performance limits caused by errors by changing the modulation frequency and amount in this manner.

In addition, the jitter tolerance test for PCI Express, specifies applying two SJs; the MP1900A supports either one or independent two SJs addition using option configurations.

Moreover, it can apply sufficient SJ of 1UI at jitter tolerance tests in the high-speed modulation area for modulation frequencies above 10 MHz.

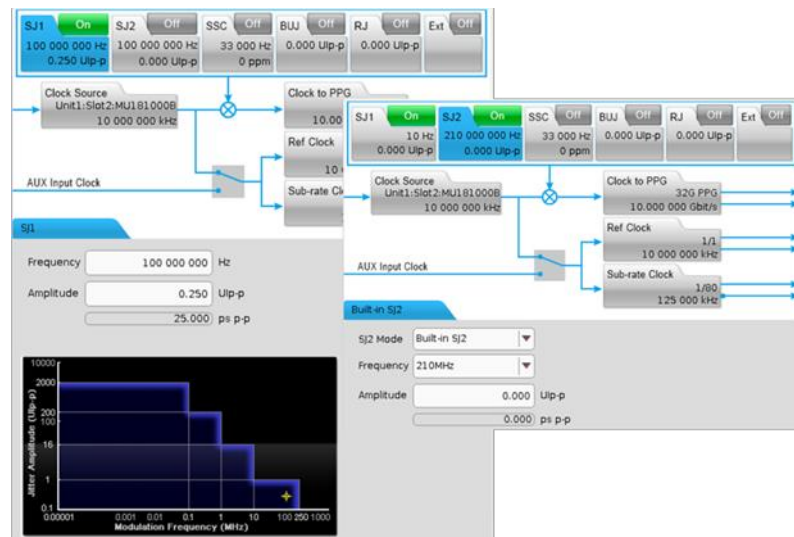


Figure 2.1.3 MP1900A SJ Setting Screen

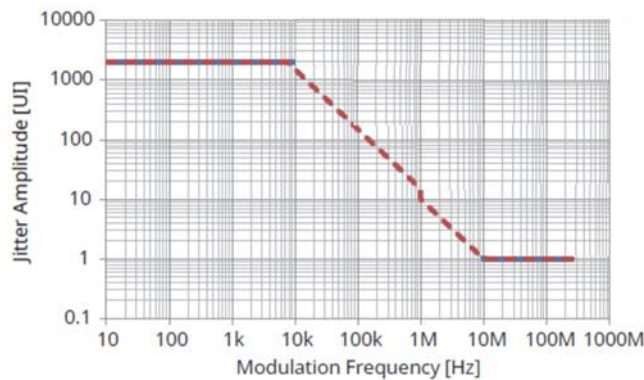


Figure 2.1.4 MP1900A SJ Mask at 32 Gbps

2.2 RJ (Random Jitter)

Random Jitter is a jitter component that is generated by noise effects that have no dependent relationship with frequency, such as thermal noise commonly occurring within systems, and it covers a wide frequency range.

For RJ, the CEI 3.0 jitter tolerance test standardizes use of a High Pass Filter (HPF) to remove RJ components within the PLL band as shown below and applies only PLL out-of-band components as the load.

2.A.3 Annex - Random Jitter Mask

To ensure that the random jitter modulation of stressed signals is above the CDR bandwidth and therefore untracked, the following filter mask shall be applied where necessary.

Figure 2-5. Random Jitter Spectrum

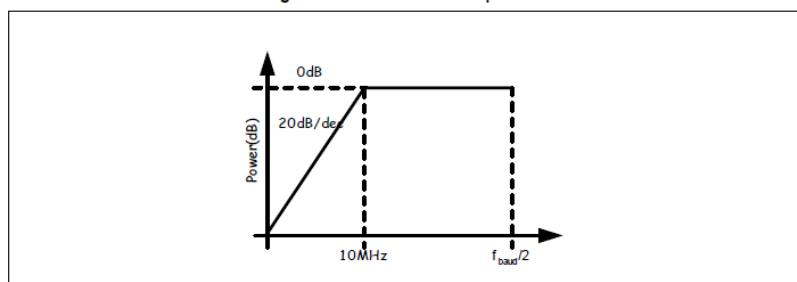


Figure 2.2.1 CEI 3.0 RJ Filter Mask

Using this standard, the HPF is set for frequency components below 10 MHz but it is necessary to apply frequency components at least exceeding the CDR bandwidth. The maximum amount of applied RJ is half the Baud rate so if the Baud rate is 28 Gbps, the applied RJ max. is 14 GHz. However, the actual CDR bandwidth does not extend to half the Baud rate, and it is usually sufficient to test a range of about 10 times the normal PLL bandwidth. Consequently, if the measuring instrument RJ band is from 100 to 200 MHz, the range required by the test will be sufficiently covered. As described in item 2.1 above, this is because jitter accumulates as the CDR bandwidth becomes wider, causing overall system instability.

The MP1900A has a built-in HPF and LPF for easy RJ injection. The built-in HPF and LPF should be used in combination to increase the reproducibility of jitter tolerance tests instead of attaching external filters.

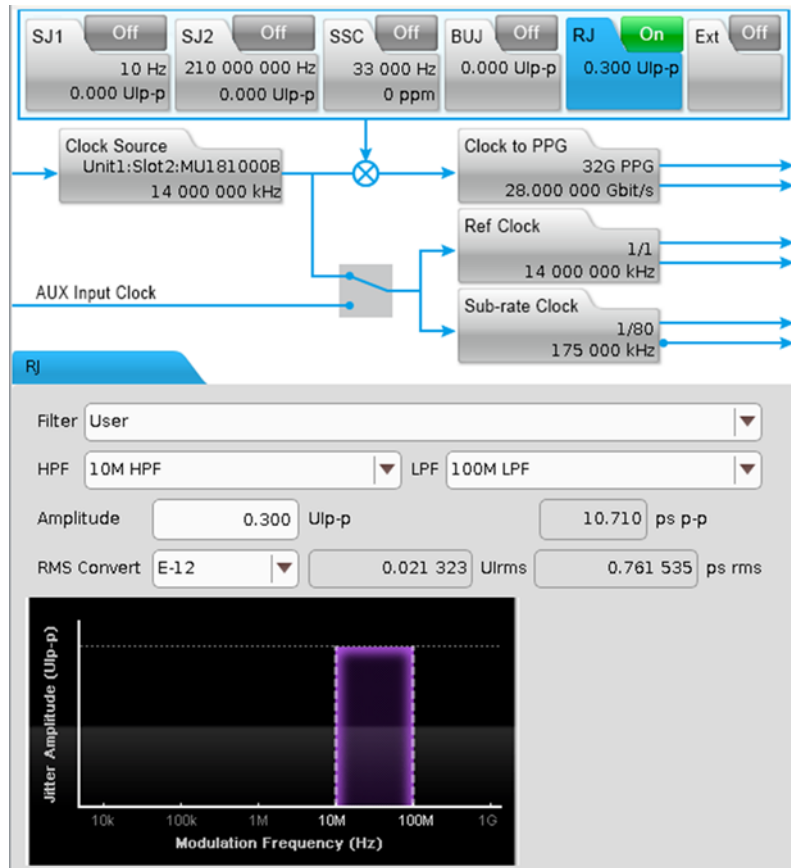


Figure 2.2.2 MP1900A RJ Setting Screen

Additionally, RJ has an MP1900A Filter setting item; when PCIe is selected at Filter, the amounts of RJ (ps rms) for the Low and High Frequency bands required by PCI Express can be set independently.



Figure 2.2.3 MP1900A RJ Setting Screen for PCIe

2.3 BUJ (Bounded Uncorrelated Jitter)

Bounded Uncorrelated Jitter is generally jitter caused by crosstalk caused by nearby Data signals. When it is generated from a measuring instrument, a PRBS signal generated from an independent clock source that is unaffected by correlation from Data signals is used as the measurement target. If a PRBS15 signal is used as the measured Data signal, it is better to use something other than PRBS15 to avoid interference. Moreover, it is best to set a value that is a multiple of the measured target bit rate to suppress interference even at the BUJ PRBS bit rate.

The CEI 3.1 standard recommends using PRBS31 as a general test pattern as well as for jitter tolerance tests using measured target Data signals. The BUJ PRBS patterns are from 7 to 11 stages with baud rates of 1/10 to 1/3 of the measurement target; the standard recommends using an LPF of 1/20 to 1/10 of the BUJ PRBS baud rate.

An example setting prescribed by the existing CEI 3.0 standard when using a 28-Gbps PRBS31 signal as the measurement target Data signal is described below. Since the measurement target is 28 Gbps, the required baud rate is from 1/10 to 1/3 of this, or from 2.8 Gbps to 9.3 Gbps; since the LPF is 1/20 to 1/10 of the BUJ baud rate, the value is set from 140 MHz to 930 MHz. Moreover, the BUJ PRBS is selected from 7, 9 or 11 stages. If PRBS 7 stages is used as the measurement target signal, it is better to use either 9 or 11 stages for the BUJ instead of using the same PRBS pattern as the measurement target.

The following table 2.3.1 shows the range of baud rate settings when applying BUJ using the MP1900A.

Table 2.3.1 BUJ Settings

Items	Value	Note
PRBS	7, 9, 11	Uses different pattern from main signal
Bit rate	1/10 to 1/3	2.8 to 9.3 Gbps (@28 Gbps)
LPF	1/20 to 1/10	140 to 930 MHz (@28 Gbps)

Table 2.3.2 MP1900A BUJ Baud Rate Setting Range

Baud rate (Gbps)	Step (kbps)
0.1 to 3.2	1
4.9 to 6.25	1
9.8 to 12.5	1

Using the previous example, BUJ baud rate for 28 Gbps is from 2.8 Gbps to 9.3 Gbps, the highest baud rate for BUJ is 6.25 Gbps. In this case, the standard specifies a setting range from 312.5 MHz to 625 MHz for the LPF. Since the MP1900A LPF used for BUJ can be selected from 500 MHz, 300 MHz, 200 MHz, 100 MHz, and 50 MHz. 500 MHz should be selected in this example. Although the BUJ pattern can be selected from any of 7, 9, 11, 15, 23, and 31 when using the MP1900A, either 7, 9, or 11 is selected based on the CEI 3.0 standard.

2.4 Half Period Jitter (F/2 Jitter)

With the recent speed increases in semiconductor bit rates, semiconductor vendors are avoiding deployment of hard-to-handle full-rate-clocks in semiconductor devices and are instead using a Selector at the final output stage and there are increasing numbers of examples using a half-rate clock (Figure 2.4.1).

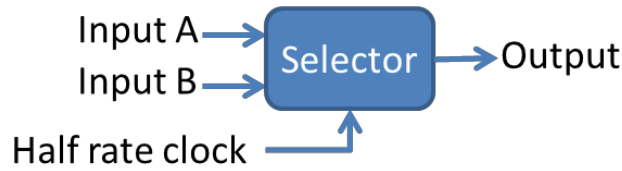


Figure 2.4.1 Selector Type Output

The general circuit shown in Figure 2.4.1 operates at the timing shown in Figure 2.4.2.

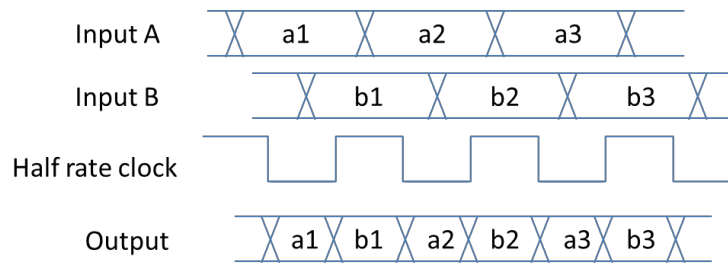


Figure 2.4.2 Selector Operation Timing

If the half-rate clock does not have a Duty of 50% at this time, the output Data cycle looks as shown in Figure 2.4.3 and the narrow and wide state is repeated at each bit. This is called Half Period Jitter (HPJ).

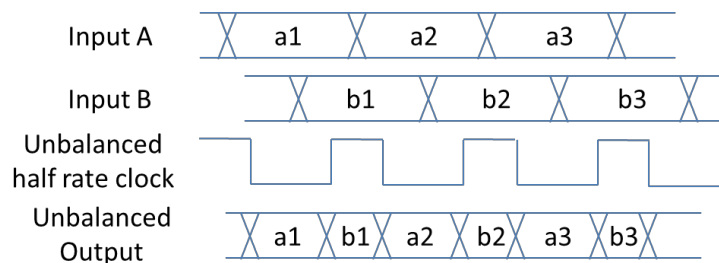


Figure 2.4.3 Selector Output when Clock Duty not 50%

The factors causing the Clock Duty change are drift in the Clock Buffer Threshold voltage in the semiconductor device as well as distortion in the Clock waveform which can be caused by inadequate bandwidth as well as other issues.

Half Period Jitter is used to confirm whether or not a signal that is output under these conditions can be received correctly by the receiver circuit.

Since the MP1900A has a function for applying HPJ on the Pulse Pattern Generator (PPG) output, it can be used to add HPJ while applying jitter types such as SJ, RJ, BUJ to create even more severe stress conditions. In determining the HPJ setting amount, to separate-out DJ (DDPWS) caused by ISI, it is first necessary to generate a 1010 Clock pattern as the Data signal, which is defined as HPJ, and then to calibrate the DJ.

3. Tips for Jitter Tolerance Measurement

Generally, jitter tolerance measurements of semiconductor devices are performed repeatedly on multiple devices while changing multiple parameters including temperature, voltage and bit rate. Excluding the changed parameters, the other test conditions must be kept the same to assure high test repeatability. This section describes the items, such as the connection cables between the measuring instruments as well as the settings themselves, to consider for performing a jitter tolerance test with high repeatability.

3.1 Cable Lengths

Figure 3.1.1 shows a typical jitter tolerance test setup.

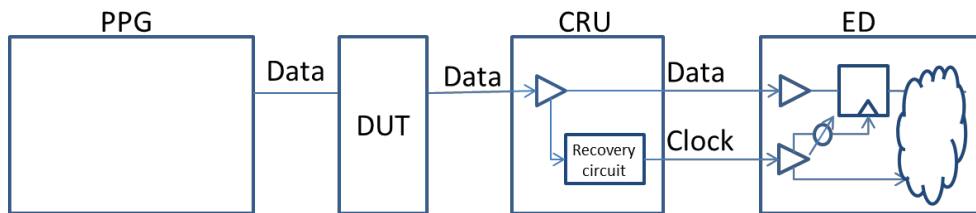


Figure 3.1.1 Jitter Tolerance Test System

The point requiring attention here is the length of the Data and Clock paths connecting the Clock and Data between the blocks. In Figure 3.1.1 these are the connections between the CRU (Clock Recovery Unit) and ED (Error Detector).

Although jitter from the transmitter side is transmitted over both the Data and Clock paths at the same timing, if there are differences in the path lengths, the phase relationship between Clock and Data drift at the receive side decision circuit (D-FF in the ED in Figure 3.1.1) causing errors to occur. To prevent errors caused by different path lengths, it is important that the length of the Data and Clock paths are the same including transmission delay times in the upstream and downstream blocks. In the example of Figure 3.1.1, it is necessary to pay attention to: 1. The lengths of the Clock and Data paths after the Data is separated into Clock and Data in the CRU; 2. The lengths of the Clock and Data paths in the ED; and 3. The lengths of the cables connecting the CRU and ED Clock and Data. If the above-described total Data path length and total Clock path length are the same, errors caused by the measurement system setup can be prevented. Since it is difficult to evaluate the length of the Data and Clock paths in the blocks from outside, measuring instrument vendors offer this length.

For details about handling of the Clock and Data cables refer to our company note on [Effect of Transmission Line Length on BER Testing, Technical Note](#).

Additionally, Anritsu also offers a Clock Recovery option that can be embedded in the ED. Embedding Clock Recovery into the ED offers a big advantage over using an external CRU.

Embedded Clock Recovery in the ED eliminates the need for users to have any knowledge about the length of the Data and Clock paths between the CRU and ED. In addition, the connections are simplified because there is no need to connect a Clock cable. Moreover, the simple cable connections cut the need for re-testing due to set-up errors and eliminate wasted time. Based on these considerations, Anritsu strongly recommends using the ED built-in Clock Recovery option for jitter tolerance tests. Figure 3.1.2 shows an example of an Anritsu jitter tolerance test system using an ED incorporating Clock Recovery circuit.

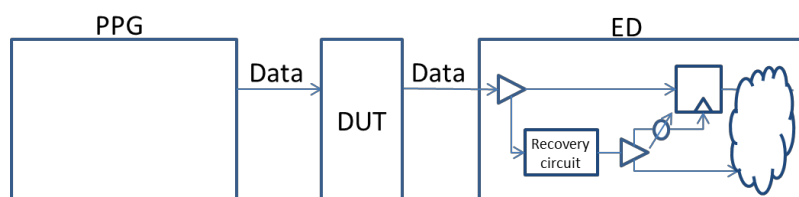


Figure 3.1.2 Anritsu Jitter Tolerance Test System with Embedded CRU

3.2 MX183000A High Speed Serial Data Test Software PL001 Jitter Tolerance Test

Anritsu provides the Jitter Tolerance Test software MX183000A-PL001 for easy implementation of jitter tolerance tests. This section explains a simple usage method. For more details, refer to the MX183000A operation manual. The screen shown in Fig. 3.2.1 opens when the MX183000A software is started. Selecting Jitter Tolerance Test at the Application Selector item and clicking the [Start] button opens the screen at the right side of Fig. 3.2.1.

Clicking the [Search Start] button at this screen searches for modules installed in the MP1900A main unit required to run the Jitter Tolerance Test software; pressing the [Connect] button after finding the modules opens the Jitter Tolerance Test setting screen for making detailed settings.

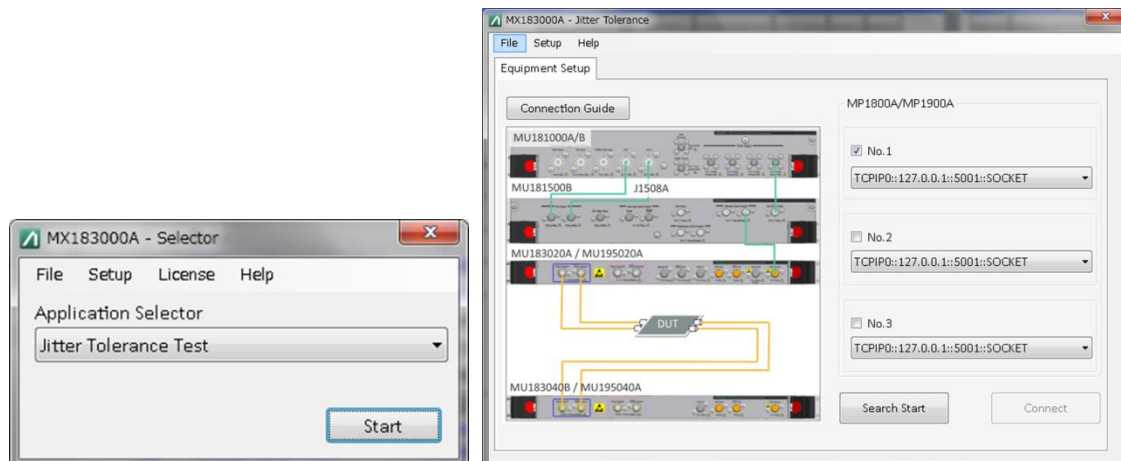


Figure 3.2.1 MX183000A Screen

The jitter tolerance test can be used to determine to what degree the actual DUT performance exceeds the standards by increasing the jitter up to the measuring instrument jitter generation limit and observing whether the DUT generates errors. One measurement parameter is the SJ modulation frequency and modulation amount, and fixed amounts of secondary background SJ, RJ, BUJ, and SSC can also be applied at measurement.

At jitter tolerance measurement, the amount of jitter is changed until the designated error condition is detected by searching. There are two search methods: Downwards from large to small values, and Upwards from small to large values. The search steps for both the Downwards and Upwards searches can be specified as either Linear using a fixed value, or as Logarithmic using a value changing at a fixed ratio. In addition, since the MX183000A software itself can be controlled by remote commands, it can be incorporated as part of automated measurement software for DUT inspection.

3.3 Equalizer

With the increasing bit rates noted at the start of this report, at the jitter tolerance test, it is necessary to consider the impact of signal degradation on the measurement results for a DUT, such as a semiconductor chip, mounted on a PC board. Even if no DUT errors occur after applying jitter from the measuring instrument, the output signal waveform of a DUT mounted on a PCB may be degraded, sometimes resulting in complete closure of the EYE signal input to the ED as shown in Figure 3.3.1.

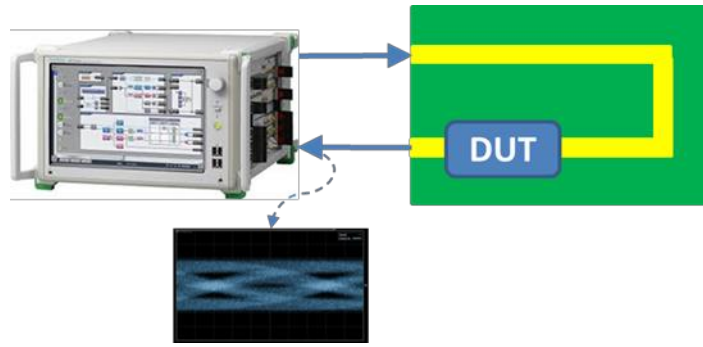


Figure 3.3.1 Closed DUT Output EYE on PCB

In these cases, even if the DUT has sufficient jitter tolerance, it is impossible to measure errors with an ED because the EYE is closed. Consequently, accurate jitter tolerance test results cannot be obtained. To get good jitter tolerance test results, it is necessary to use an Equalizer to correct the effect of waveform distortion caused by PC board transmission paths and other factors.

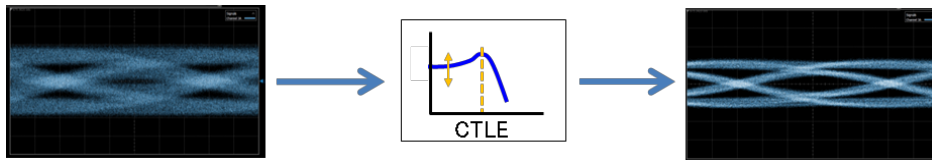


Figure 3.3.2 DUT Output Waveform after Equalizer

To correct the effect of distortion caused by the PC board transmission path and measure error using the ED, a CTLE is incorporated in the ED; it can be adjusted between 0 and 12 dB for signals in the 8 to 10 Gbps, 16 to 20 Gbps, and 25 to 28 Gbps bands.

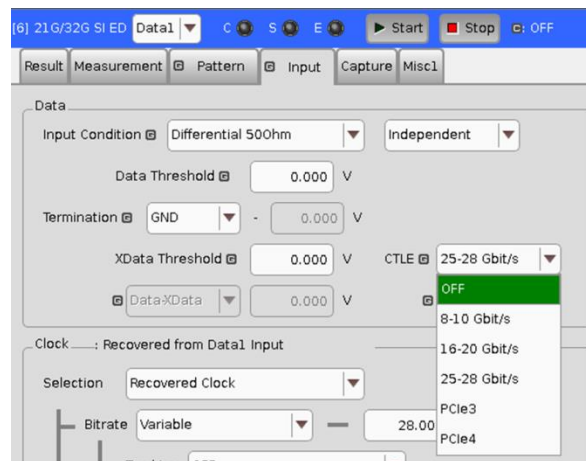


Figure 3.3.3 MP1900A ED CTLE

3.4 Amplitude Noise Interference

Reflection and distortion caused by transmission-path impedance mismatching can be observed in the High and Low baselines of digital signals. These reflections and distortion are seen as baseline noise in the Eye Pattern. Standards for PCIe, Thunderbolt, Ethernet, etc., specify transmission tests using a stressed waveform with applied amplitude noise and phase jitter. With a built-in function for applying amplitude noise, the MP1900A makes it easy to generate white noise, common mode noise, differential mode noise, etc.

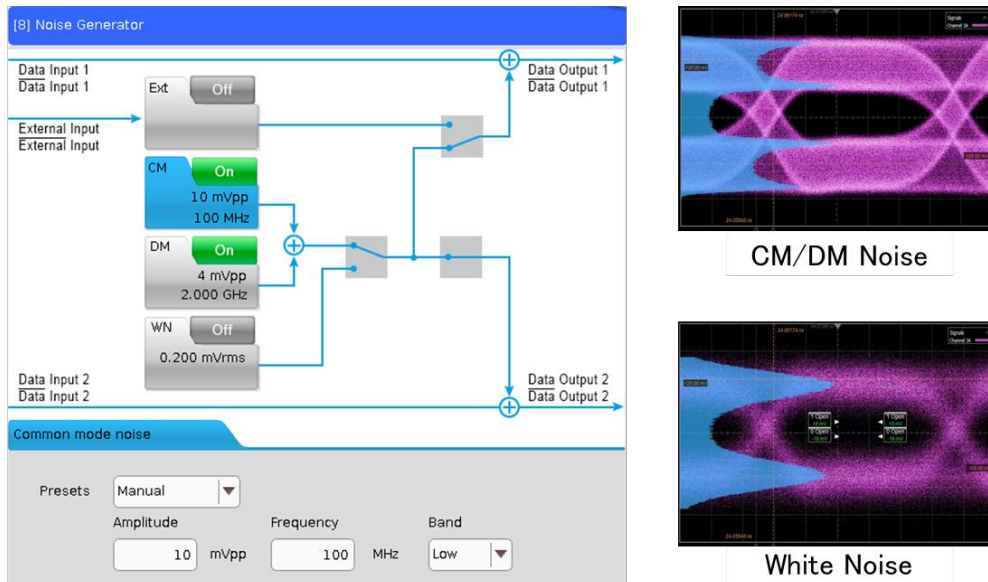


Figure 3.4.1 Amplitude Noise Interference

4. Summary

This Application Note has explained the complex meaning of jitter and how jitter can be generated using the MP1900A. It has also explained jitter tolerance measurement methods using the MP1900A. Anritsu continues to offer measurement solutions meeting its customers' business needs.

References

- Implementation Agreement OIF-CEI-3.1 February 18, 2014
- [Effect of Transmission Line Length on BER Testing \(Technical Note\)](#)

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